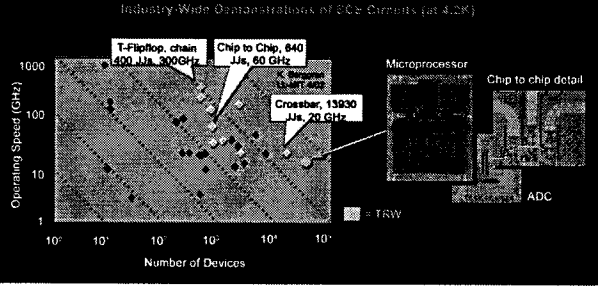
HTMT

# SUPERCONDUCTING ELECTRONICS PROCESS IMPROVEMENT

## Aggressive SCE Development Continues




- 60 Gb/s world record chip to chip SCE logic communication
  Includes 60 GHz psuedo-random binary sequence (PRBS) generator
  Featured in NATURE online (www.nature.com) May 8, 2002
- 300 GHz digital divider measures world's fastest SCE foundry process
- Record of Ist pass success measures processes and discipline

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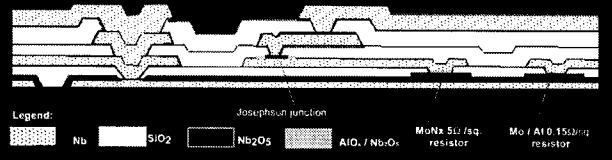



8 kA/cm² Process Features

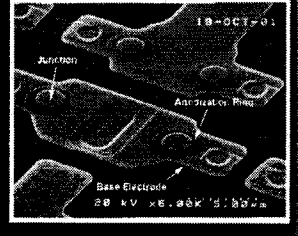
- Junction anodization
- Three wiring levels and one ground plane
- Two resistor values (5.0 and 0.15 Ω/sq.)
- 14 masking step

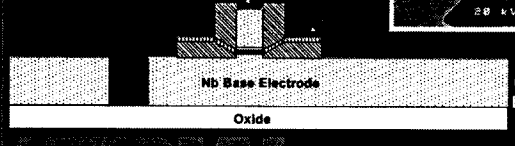
Design Rule Features

- 1.0 μm minimum feature contacts)
- 1.25 μm junctions
- 2.6 μm wire pitch

## Anodized Junctions

SEM Photograph of 300 GHz Static Divider Stage




Cross section after base electrode etch

## Nb Superconductor IC Fabrication Technology Development Roadmap

| | Nb Technology | | | | | SIA CMOS |
|---|---|---|---|---|---|---|
| *Year* | 1998 | 2000 | 2002 | 2004 | 2005 | 1992 |
| *Minimum feature* | 1.5 μm | 1.0 μm | 1.0 μm | 1.0 μm | 0.75 μm | 0.5 μm |
| *Minimum junction* | 2.5 μm | 1.75 μm | 1.25 μm | 1.00 μm | 0.75 μm | N/A |
| *$J_c$ (A/cm²)* | 2000 | 4000 | 8000 | 12000 | 20000 | N/A |
| *Number of masks* | 12 | 12 | 14 | 14-18 | 18 | ~ 20 |
| *Resistors* | 2 | 2 | 2 | 2 | 2 | N/A |
| *Metal line pitch* | 4 μm | 3 μm | 2.6 μm | 2.4 μm | 2 μm | 1.2 μm |
| *Metal interconnect levers* | 4 | 4 | 4 | 4-6 | 6 | 3 |
| *Planarization* | no | no | partial | yes | yes | yes |
| *Max. defects per cm²* | 2 | 2 | 1 | .2 | .1 | .1 |
| *Wafer starts per month* | 12 | 12 | 12 | 120 | 240 | 20K |
| *I/O count* | 128 | 128 | 128 | 640 | 1200 | 500 |
| *$F_{max}$ (GHz), divider freq.* | 150 | 210 | 300 | 370 | 475 | 1 |
| *Processor Clock (GHz)* | 30 | 40 | 60 | 80 | 100 | 0.2 |
| *Gate Density (gates/cm²)* | 6K | 8K | 16K | 32K-64K | 128K | 300K |